

HX5000 Standard Cell ASIC Platform

GENERAL DESCRIPTION

The Honeywell HX5000 Platform ASICs are manufactured on the Honeywell's fully QML Qualified 150nm CMOS Silicon on Insulator technology using a cell-based library and advanced ASIC design methodology. The design and manufacturing flow supports ASIC development from RTL through delivery of tested ASICs. This high density ASIC technology supports a full range of radiation hardness requirements.

Honeywell's S150 150 nm Silicon on Insulator (SOI) process enables ASICs with approximately 15 million usable gates. This is achieved using a fully planarized 6 or 8-layer metal process. HX5000 is designed for use over the full military temperature range while operating in harsh radiation environments. The S150 technology is designed to withstand extremely high levels of Total Dose radiation hardness. The HX5000 ASIC library, flip-flops and SRAM cells are designed for extremely low static and dynamic Soft Error Rates (SER).

The ASIC development methodology that supports these complex ASICs is based on Synopsys toolsets. This robust design flow supports flexible design handoffs with multiple entry points including specification, RTL, or synthesized gate level netlist.

Design For Test (DFT) is an integral part of this design flow.

Each HX5000 design is based on the proven ASIC Library of standard logic elements, module compiler cells, configurable RAMs, Phase Lock Loops (PLL) and selectable I/O cells.

Designers can choose from a wide variety of I/O types. High speed and standard bus interfaces such as PCI, LVDS, SSTL2, HSTL and LVPECL buffers are available. A high speed SerDes interface provides 3.1875 Gb/s per lane performance. Standard CMOS I/O cells include buffers with multiple drive strengths, three-state capability, and pull-up/pull-down resistors. The HX5000 product family supports 1.8V and 1.6V core operation, 1.6V (LVPECL), and 1.8V, 2.5V, and 3.3V I/O operation.

Many package types are available including CQFP, LGA and FC-LGA including column attach for LGA packages.

Honeywell implements QML Qualified reliability and screening procedures that are fully compliant with Class V requirements.

FEATURES

- Fully QML Qualified ASIC Flow
- Fabricated on S150 Silicon On Insulator (SOI) CMOS
- 150 nm Process
- Proven Radiation Hardness
- Total Dose Hardness: 1×10^6 rad (Si)
- Dose Rate Upset Hardness: 1×10^{11} rad(Si)/s
- Dose Rate Survivability: 1×10^{12} rad(Si)/s
- No Latch-up
- Low Power
 - 15 nW/MHz/Gate (1.8V)
 - 12nW/MHz/Gate (1.6V)
- I/O Options:
 - 1.8V/2.5V/3.3V CMOS
 - Cold spare
 - PCI
 - 1.8V/2.5V/3.3V LVDS Tx
 - 2.5V, 3.3V LVDS Rx
 - 1.6V, 1.8V LVPECL
 - SSTL2 Class I and II
 - HSTL
- 4 & 8 Lane SERDES
 - 1.0 – 3.1875 Gb/s per lane
 - Supports 8b10b protocols
- Wide selection of Single- and Dual-Port Drop-In SRAMs
 - High Density SRAMs
 - Custom SRAMs available
- 50MHz - 1200MHz PLL
- ASIC Design Methodology based on Synopsys tool set
- Package Signal I/O count:
 - Up to 968 for wire bond
 - Up to 1248 for flip chip
- Operating Voltages
 - 1.8 V or 1.6V Core
 - 1.8V, 2.5V and 3.3V I/O
 -
- Operating Temperature Range of -55°C to +125°C

TECHNICAL DESCRIPTION

S150 SOI CMOS Technology Description

HX5000 ASICs begin with a base 150-nanometer silicon-on-insulator CMOS (S150) technology. SOI CMOS offers advantages for high-performance circuits in radiation environments that are not attainable in standard bulk CMOS. The devices are fabricated in a thin film of silicon above the oxide insulator on top of a standard silicon wafer. This technology has a proven history of resistance to Single Event Upset (SEU), Dose Rate radiation and is immune to latch-up.

Reduced Power Consumption

- SOI technology offers lower capacitance than bulk CMOS, achieving lower power operation.
- 1.8V operating voltage of the core and I/O cells.
- 1.6V core operation and library now available.
- High speed serial output cells and macros such as SerDes reduce number of output drivers.

TECHNICAL PARAMETERS

HX5000 Characteristics	Value
Maximum Routable Gates (1)	~15 Million
Maximum Package I/O Count	Wire Bond Flip Chip
Layers of Metal	6 or 8
Operating Voltage (Core)	$1.8 \pm 0.15V$, $1.6 \pm 0.1V$
Operating Voltage (I/O)	$1.8 \pm 0.15V$, $2.5 \pm 0.2V$, $3.3 \pm 0.3V$
Typical Intrinsic Delay-2 Input NAND (fan out =2)	80 ps @ 1.8V
Typical Power Dissipation, $\mu W/MHz/Gate$ 20% Data, 200% Clock Activity Rate	0.015 @ 1.8V 0.012 @ 1.6V
Operating Temperature	-55°C to 125°C
ESD (Human Body Model)	>2000 Volts

(1) The number of routable gates is dependent on routing densities, amount of embedded RAM, package type and I/O quantity.

RADIATION-HARDNESS RATINGS

Parameter	Limits	Units	Conditions
Total Dose	1×10^6	Rad(Si)	
Dose Rate Upset	1×10^{11}	Rad(Si)/s	Pulse Width < 20ns
Dose Rate Survivability	1×10^{12}	Rad(Si)/s	Pulse Width < 20ns
Neutron Fluence	1×10^{14}	N/cm ²	1MeV equivalent energy

SINGLE EVENT SOFT ERROR RATE(1)(2)(3)

Parameter	Limits - Static	Limits - Dynamic F=100MHz	Units
Registers/Latches (4)	$\leq 7 \times 10^{-14}$	$\leq 1 \times 10^{-11}$	Upsets/bit-day
SRAM (Single Port)	$\leq 2 \times 10^{-11}$	$\leq 6 \times 10^{-11}$	Upsets/bit-day
SRAM (Dual Port)	$\leq 1 \times 10^{-13}$	$\leq 7 \times 10^{-13}$	Upsets/bit-day
High Density SRAM (DP) (5)	$\leq 1 \times 10^{-7}$	$\leq 2 \times 10^{-7}$	Upsets/bit-day

(1) There are multiple types of registers with different SER ratings.

(2) Solar minimum, geo-synchronous orbit, 100 mils aluminum shielding under worst-case operating conditions for voltage, temperature and memory operating conditions (e.g. static or dynamic operation).

(3) Error rates for single port and dual port SRAM are dependent on configuration. Limits shown are for 2048x32 for 1.8V nominal VDD core.

(4) Static=SEU4 register, Dynamic=SEUT register

(5) Projected values.

RADIATION CHARACTERISTICS

Total Ionizing Dose (TID) Radiation

The S150 SOI process technology provides protection against TID effects by reducing charge accumulation and leakage currents in the circuit elements. The HX5000 cells radiation hardness assurance TID level was qualified by ^{60}Co testing, including overdose and accelerated annealing, per MIL-STD-883 Method 1019. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Dose Rate Transient Radiation

Dose Rate Transient radiation induces high current transients that can lead to circuit upset. The S150 process minimizes the impact of Dose Rate transients through reducing charge accumulation. Additional measures including specialized power bussing and current control techniques are used to minimize the effects of the radiation.

Neutron Irradiation Damage

SOI CMOS is inherently tolerant to damage from neutron irradiation. ASICs meet functional and timing

specifications after exposure to the specified neutron fluence.

Single Event Upset (SEU)

Single event upset radiation events induce localized charge in the circuits. These can cause a change of state in elements like flip flops, latches and embedded RAMs. The SOI CMOS process limits the amount of charge accumulation, thus improving performance. The HX5000 library contains several types of storage elements, including registers and embedded RAM, which are designed to be immune to different levels of single event radiation.

Latch up

The HX5000 Library elements will not latch up under any conditions including the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SOI substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR-type latch up structures.

HX5000 LIBRARY

HX5000 library contains over 690 standard cells with a broad array of cell types. Many logic functions have multiple versions available to allow for trade-offs of radiation tolerance, speed, power consumption, and I/O drive strengths. Flip flops and memory cells are available in several SEU levels to support different radiation requirements.

The library also contains a wide range of single and dual port embedded SRAMs and mixed signal macros such as the PLL.

Embedded SRAMs

Honeywell provides a wide selection of SRAMs to embed into your design. This library of predefined macro cells includes both single port and dual port SRAMs. The sizes range from 256 x 8 up to 16,384 x 40 with the inclusion of 9 and 33 bit configurations for designs needing single bit parity. Typical access times range from 1.5ns to 3 ns.

Honeywell also provides a service to create custom RAMs for unique applications as well as special configurations of single port specialty SRAMs, high density dual port SRAMs (~50% the size of the standard dual port SRAM) and register files. See the HX5000 Databook for complete information.

HX5000 I/O OPTIONS

Description	Operating Voltages	Max Operating Frequency	Features
CMOS	1.8V, 2.5V, 3.3V	200 MHz (1)	Cold Spare option
PCI	3.3V	33MHz / 66MHz	
LVDS	1.8V(Rx only), 2.5V, 3.3V	500 Mb/s (1)	Cold Sparing
SerDes	1.8V	3.1875 Gb/s per lane	4 & 8 channel macro cell
HSTL	1.8V	Up to 250 MHz (1)	Class I & II, Input, Output
SSTL2	2.5V	Up to 250 MHz (1)	Class I & II, Input, Output and Bi-pad
LVPECL	1.8V, 1.6V	1.2 GHz(1.8V) 200 MHz(1.6V)	Input only, AC Coupled

Notes:

(1) I/O buffer operating speeds limited by external board design and loading.

SERDES

To support high speed data communication needs, 4 and 8 channel SERDES (Serializer/Deserializer) macros are available. The SERDES implements the actual serialization and deserialization of the data, Clock generation, and Clock and Data Recovery of 8b10b encoded data.

The SERDES I/O macro-cell can transmit and receive data at rates of 1 - 3.1875 Gb/s per channel. It includes features to maximize the quality of the data transmission. To improve signal integrity and Bit Error Rate (BER), the transmitter has 8-level programmable output drivers and the receiver has 8-level equalization. An integrated PLL provides the necessary accuracy and programmability of the internal clocks.

SERDES is designed to support 8b10b encoded protocols such as Gigabit Ethernet, Serial Rapid IO, and Fibre Channel protocols.

SERDES Applications and Networks

The SERDES macro cells are designed to support 8b10b encoded high speed serial communications including point-to-point and networking applications. When embedded in an HX5000 ASIC with the user's synthesized protocol functions, the SERDES macrocell enables Gigabit Ethernet, Fibre Channel and Serial Rapid IO endpoints and switches. Custom

protocols can also be implemented making this combination a powerful tool to optimize communication performance.

PLL

The HX5000 library includes multiple PLL macro cells. The PLL macro cell operates up to 1200 MHz. It contains on-chip filtering and loop filters, a lock detect indicator and can be powered down.

Primarily used for clock phasing and clock multiplication. It can be used to cancel clock buffer delays in larger digital ASICs or to synthesize high speed clocks.

DEMUX (1.8V only)

The HX5000 Library includes DEMUX macrocells.

- 1:8 or 1:16 de-multiplexing
- Asynchronous reset of all internal registers
- High speed, capable of handling 1.5 Gbps

The DEMUX can be used to convert a high speed Non-Return-to-Zero (NRZ) serial data signal into an 8-bit or 16-bit parallel data signal using a reference clock aligned to the data and providing a data ready clock on the output. Thus, the DEMUX will be used primarily as an augmentation to high speed inputs such as the LVPECL Input buffer.

ASIC METHODOLOGY AND CAD TOOLS

The design flow infrastructure for HX5000 ASICs has been developed by Honeywell and Synopsys. This design environment includes:

- Synopsys EDA tools for designing and verifying complex ASICs.
- A flexible set of front-end and back-end design services from design teams expert in the implementation of advanced ASICs and the HX5000 design flow.
- Qualified standard-cell libraries supporting both rad-hard and rad-tolerant designs.

ASIC Development Flow

The ASIC development flow processes a design from the ASIC specification through tested ASIC delivery. The flow is configured to support preliminary synthesis and place and route to converge on an optimized design that meets all the performance constraints. The requirements associated with

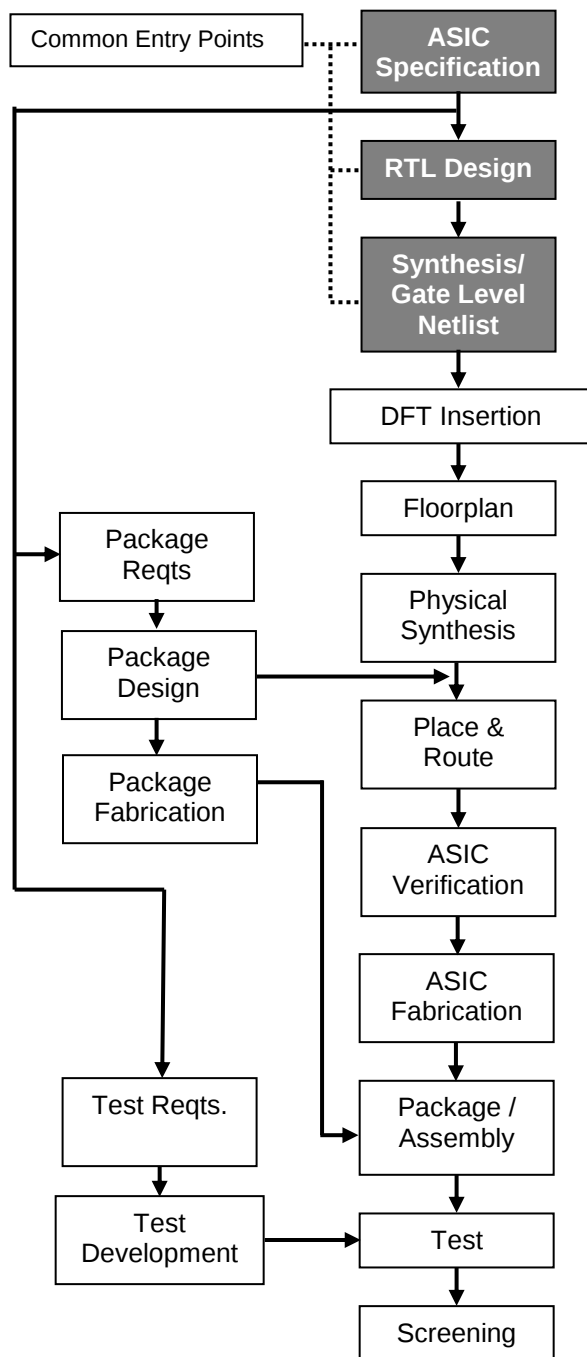
packaging and test are also addressed as part of the ASIC development.

Implementation within the ASIC flow is controlled by a Honeywell configured version of the Synopsys Lynx environment. This allows for repeatable, re-usable flow steps sharing best-practices throughout the design flow.

Design For Test (DFT)

Honeywell has integrated Design For Test (DFT) into the HX5000 ASIC Development Flow. It encompasses Memory Built In Self Test (MBIST), Boundary Scan, and SCAN. DFT insertion supports ATPG generation for standard stuck-at faults, as well as transition delay based faults. Test vector generation for manufacturing defects is included in the default flow. Additional support is available for customer based functional vectors and testing at speed for most architectures. The DFT flow is supported by tools from Synopsys, Mentor Graphics, and Credence.

ASIC Development Flow Diagram

**DFT****Memory BIST Insertion into RTL**

Memory BIST collars around the embedded RAMs in the RTL design. Inserts a top level control system utilizing an 1149.1 JTAG TAP, inserts IO boundary-scan, and runs MBIST tool verification

Synthesis

The scan control structures are inserted. Perform initial ATPG (Automatic Test Pattern Generation) scan vector generation.

Physical Synthesis

Create logical order of the scan chains on the physical placement of the cells.

Post Route Test Vector Generation**Scan Vector Creation & Simulation**

Generate ATPG stuck-at and transition delay test vector sets and verification test benches.

Memory BIST Vector Creation & Simulation

Simulations to validate the correct functionality of the TAP controller and boundary-scan, and to validate access to and basic functionality of the MBIST controllers.

DC Vector Creation/Simulation**Functional Vector Creation/Simulation****Vector Verification**

Perform basic verification that the vector files produced to test an ASIC meet tester compatibility requirements.

Vector Translation

Convert industry standard formats (WGL & EVCD) into a format that is compatible with Honeywell testers.

PACKAGING

Honeywell can provide a wide variety of single chip packages for HX5000 ASICs. The primary form factors are ceramic quad flatpacks (CQFPs) up to 352 pins, and ceramic land grid array packages (LGAs) up to 1761 pins. QML-qualified solder column attach is available for LGA packages. Contact Honeywell for the latest column attach details. Most packages are designed to conform to JEDEC standard outlines.

Honeywell can personalize standard package outlines to accommodate a variety of die footprints, pin assignments, or routing requirements. Honeywell can also design custom single chip or multi-chip modules.

Honeywell's package designs meet a wide range of thermal, electrical, and mechanical performance requirements. Thermal resistances (junction-to-board) of approximately 1 °C/Watt are typically achieved for 15mm die sizes in LGAs or CQFPs. Honeywell can provide thermal or electrical modeling of package characteristics as part of the package design.

Package Construction and Assembly Processes

Our standard ceramic packages utilize wire-bond assembly that are hermetically sealed, screened and qualified to MIL-PRF-38535 Class Q or V requirements. The table below summarizes the basic materials and assembly methods for Honeywell's qualified, wire bonded ceramic packages.

HERMETIC CERAMIC PACKAGE PARAMETERS

Feature	Description	Feature	Description
Package Body	90% Alumina (Al ₂ O ₃)	Leads, Seal Ring	Kovar (Fe-Ni-Co) with CuAg braze
Internal Metallization	Tungsten or Molybdenum	Lid	Kovar or Ceramic
Metal Layers	Up to 21 layers for signal routing and Power\ Ground distribution	Die Attach	Cyanate ester
External Metallization	Nickel-gold plating	Wirebond	Ultrasonic Al Wedge Bond
		Hermetic Seal	AuSn solder seal

FLIP CHIP PACKAGING

For ASICs with very high I/O count, high power dissipation or performance requirements, flip chip packages are available. This technology extends the available pad count to well over 1000 per die, and also improves the electrical, thermal, and radiation performance of the package ASIC. Packages for flip chip devices are typically ceramic land grid arrays, and do not require a hermetic lid seal. Contact Honeywell for further details.

TEST CAPABILITIES

Honeywell HX5000 test capabilities include wafer and packaged part level testing supporting Class V screening.

RELIABILITY

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in the early 1990's.

Using this proven approach Honeywell will assure the reliability of the products manufactured on the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDDB, hot carriers, bias temperature instability, radiation)
- Utilizing a structured and controlled design process
- Statistically controlling wafer fabrication process with a continuous defect reduction process
- Individual wafer lot acceptance through process monitor testing (includes radiation testing)
- Using characterized and qualified packages
- A thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

QUALIFICATION AND SCREENING

The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot-based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests - 1000 hours at 125C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

This document contains an overview of the features and capabilities of the HX5000 Standard Cell ASIC Platform. For a full description of the specification and performance, refer to the HX5000 Databook and User Manual.

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